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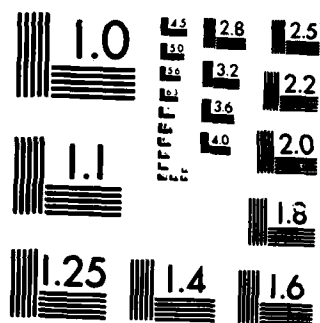
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LAIRTS PIXEL DATA FORMATTER

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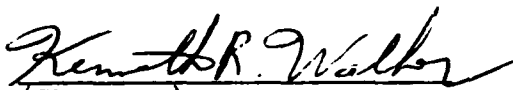
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Synchronized PCM

SUMMARY

The Oklahoma State University Electronics Laboratory designed a system to assemble the asynchronous data from a pixel array together with the required housekeeping (HSKP) data and format these data into a bit stream for magnetic tape recording. This report covers in detail the design of the pixel data storage system and its entry into the bit stream. The format requires a minor frame length of 132 words and a subframe length of 128 frames. There was very little available information on the amount of HSKP data that would be required. However, very simple modifications to the formatter would accommodate extra HSKP words and they are relatively easy to format.

*Keywords: multiplexing; analog to digital converter;
precision bit shift out shift registers;
focal plane arrays.*

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1.0 INTRODUCTION

The primary objective of the Electronics Laboratory was to develop a system to store the data outputs from a 128×128 array of gallium doped silicon direct readout pixels and format these data together with the required timing and other housekeeping (HSKP) data into a synchronized PCM bit stream for magnetic tape recording. The focal plane array (FPA) was to be composed of four 64×64 panels of 4 mil pixels. The analog data outputs from these pixels were to be multiplexed into eight, 14-bit A to D converters and parallel-entered into 8 associated parallel in/serial out shift registers all internal to the focal plane array.

It was required that the total array be sampled in 320 milliseconds or less. The complete array was not to be sampled more often than once per second. The normal scan rate would vary anywhere from one scan per second to one scan per three-hundred seconds.

Provision also had to be made to record the fast scan of an 8×8 pixel array from any one of the four 64×64 panels upon a command from the master controller. In this mode of operation the address of the 64×64 panel from which the 8×8 fast scan was taken and the address of the upper left pixel of the 8×8 array was to be furnished to the data formatter from the FPA. These addresses were to be inserted in the HSKP data words together with the universal time and pointing angles to facilitate data reduction.

2.0 Theory of Operation

2.1 Data Acquisition

A somewhat detailed block diagram of the data acquisition system is shown in Figure 1. The following is a description of the operation. A command from the master control signals the FPA to start a "data take". Analog data from the pixels are then converted into digital data eight pixels at a time and parallel entered into eight shift registers. A "data ready" from the FPA then signals the formatter to simultaneously empty these eight registers in serial bit streams into a storage buffer. When all data has been taken and transferred into storage, a "buffer full" flag signals the formatter to clock data out during the next major frame. See normal scan format in Figure 2. Universal time, pointing angles and other HSKP data are subcommutated in two words of the minor frame.

2.2 Formatter Timing

A schematic diagram of the data formatter timing circuits is shown in Figure No 3. Y 101 is a 1 MHz crystal-controlled oscillator which is counted down in the first half of a dual 4-bit binary counter (IC 101) for a 250 KHz bit clock for the output bit stream. The second half of this IC together with a three-input AND gate provides a word clock of 14 bits per word. The word clock is then fed to binary counter, IC 106, which resets itself through a two-input AND gate for a minor frame sync pulse and a minor frame length of 132 words. The minor frame sync pulses are then counted by another binary counter IC 110 which resets itself with Q8 output to give a major frame length of 128 minor frames. The binary outputs of this counter are parallel entered into a 7-bit shift register(IC 111) for subframe identification. The frame sync word is programmed on the parallel inputs of IC 112 & 113 . It and the ID word are both parallel-entered with the minor frame sync pulse and are clocked out together by feeding the serial output of the ID register into serial input of the frame sync generator. Since the subframe ID requires only seven bits of the fourteen bit word, seven flag bits could be clocked into the serial input of the ID register.

The analog data from the pixels are converted eight pixels at a time into fourteen bit digital data in the normal scan of the 128 x 128 array. The A-to-D outputs are then parallel-entered into eight shift registers for simultaneous serial shifting into storage buffer. A "data ready" pulse is then sent to the formatter to initiate the transfer.

The bit clock for this transfer is derived from the Q1 output of a binary counter (IC 105). This is a 250 KHz clock, which is counted down from the 1 MHz crystal

controlled oscillator through Q1 of IC 101. At the beginning of a data readout the 500 KHz clock to IC 105 has been disabled by a high output from the three input AND gate (IC102B) applied to pin 2 of OR gate IC 104A. A "data ready" pulse from the FPA resets this counter and thus enables the clock input for 14 cycles of the clock output to the FPA serial-output shift registers. These same clock pulses are also applied to the selected buffer address counter through IC 120. Upon completion of the fourteenth pulse IC 102B output goes high again disabling the counter input. This gate output also is sent to the FPA to signal the transfer is complete and formatter is ready for the next readout.

2.3 Pixel Data Storage

The data storage system is comprised of two identical RAM systems with their associated address counters (See Figure 4). Each memory consists of fourteen 2048 x 8 CMOS static RAM chips. Pin numbers except for the \bar{E} of all RAMS are tied in parallel. The input/output pins are all from one chip of eight 3-state buffers outputs and to another 3-state buffers inputs. The inputs of the input buffer chips of both memory systems (IC 208 & IC 215) are tied in parallel as are the outputs from the output buffers, IC 211 & IC 214. Inputs 1 & 2 of both inputs are from a dual 4-channel demultiplexer (IC 201) having two binary control inputs, A & B. The two binary input signals connect 1 of 4 pairs of input signals to the outputs. This provides a means of selecting two outputs from any one of the 64 x 64 pixel quadrants to go into inputs 1 & 2 of the memory buffer for a fast scan of an 8 x 8 array from the selected quadrant.

A set-reset flip-flop, IC 119A, controls the memory input/output 3-state buffers and RAM address switching. A "data start" pulse triggers one-shot, IC 118B, which resets the RAM buffer that has been receiving data and toggles the control flip-flop to read the data out from that buffer.

The eight RAM outputs are fed into eight 14-bit serial-in /parallel out shift registers. In the normal (128 x 128 array) mode of operation when the selected memory is full the associated RAM address system provides a "memory full" signal to pin 10 of IC 120 (Figure 3.) This sets the Q of a reset flip-flop, IC 119B, high which puts one input (pin 5 of IC 109) of a four-input AND gate high. This signals the formatter that pixel data is ready to be clocked into the bit stream. The output of this gate provides the pixel data readout start pulse in each minor frame. For the normal scan the readout must start on frame zero of the major frame. This is insured with the input to pin 2 of the AND gate which is controlled through a two input OR gate. Pins 5 & 6 of IC 104B are controlled by a dual set-reset flip-flop, IC 108. Pin 5 of the OR gate is set high by

the major frame sync and reset low on minor frame word 8 through IC 108A. This allows the data readout to start only on frame zero. Pin 2 of the AND gate must be returned high after major frame sync is acquired in order to maintain operation through succeeding frames. This is accomplished through pin 6 of the OR gate with the second set-reset flip-flop, IC 108B. Its Q output was reset with the major frame sync pulse and is returned high through IC 104C by the data readout start pulse. The Q output of IC 108B also triggers one-shot, IC 118B, at this time through IC 117B and IC 104D to reset the RAM buffer address and toggle the buffer control flip-flop from write to read.

The minor frame word in which the readout starts is selected through pin 3 of the start gate, IC 109. This input is controlled by a decade counter with 10 decoded outputs (IC121) which counts the word clock. Each output goes high in sequence immediately following the word clock input. The word clock is also applied to pin 4 of the start gate. Therefore the actual start pulse appears at the trailing edge of the word selected at pin 3. This start pulse resets a second decade counter with 10 decoded outputs, IC 116 through OR gate IC 114A and sets Q of IC 115 high. The counter will now be advanced by the word clock through IC 107C. This gate output word clock is also used to parallel-enter data from the serial-to-parallel converter outputs into the final pixel data output shift register.

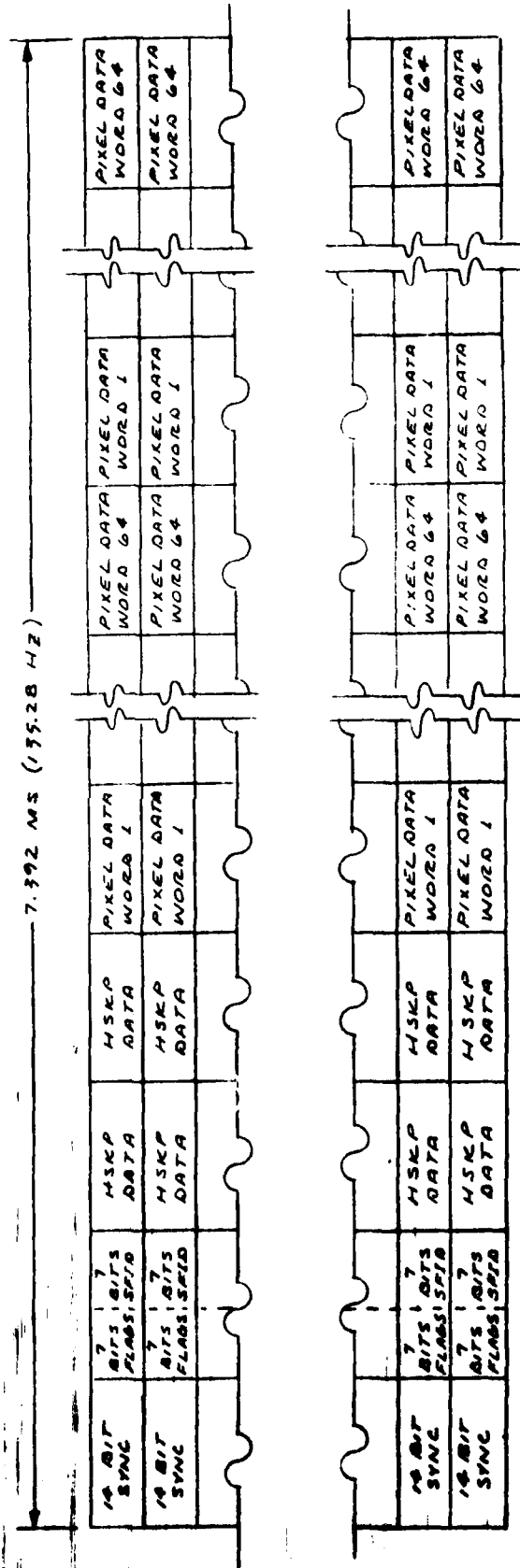
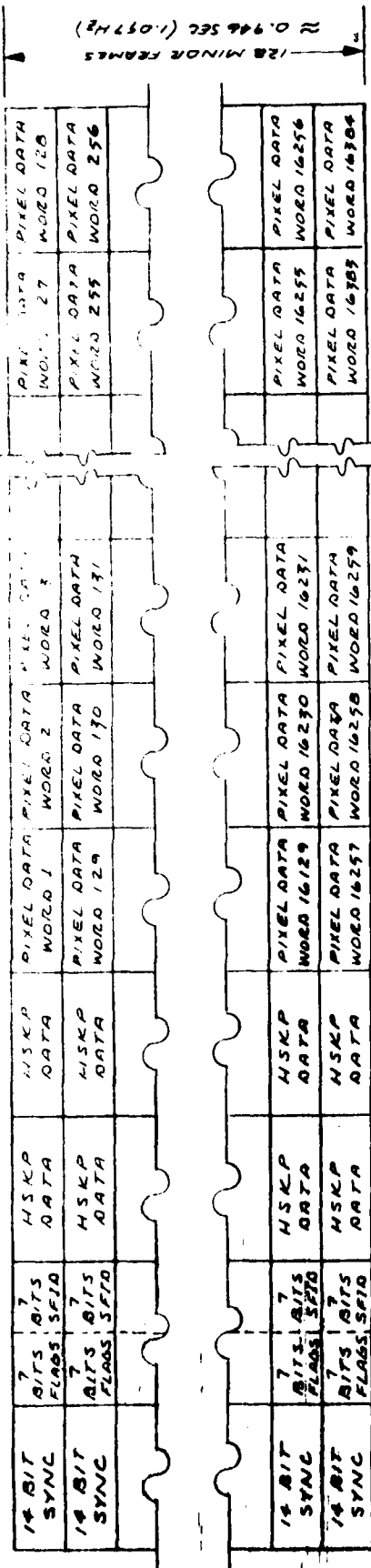
The "zeroes" output of this counter gates the bit clock to the counters and the RAM address counter through IC 102C. It also latches the transferred data into each converter's output storage and provides the output enable to the No 1 serial parallel converter. This output data is parallel-entered into the output register just inside the trailing edge of the output enable pulse. The No 2 through the No 8 converter outputs are then enabled in sequence and parallel-entered into the output register in the same manner. The counter then resets itself with No 8 output to repeat the process for eight more words. The minor frame sync resets IC 115 to stop the process at the end of each minor frame until enabled again on the selected word.

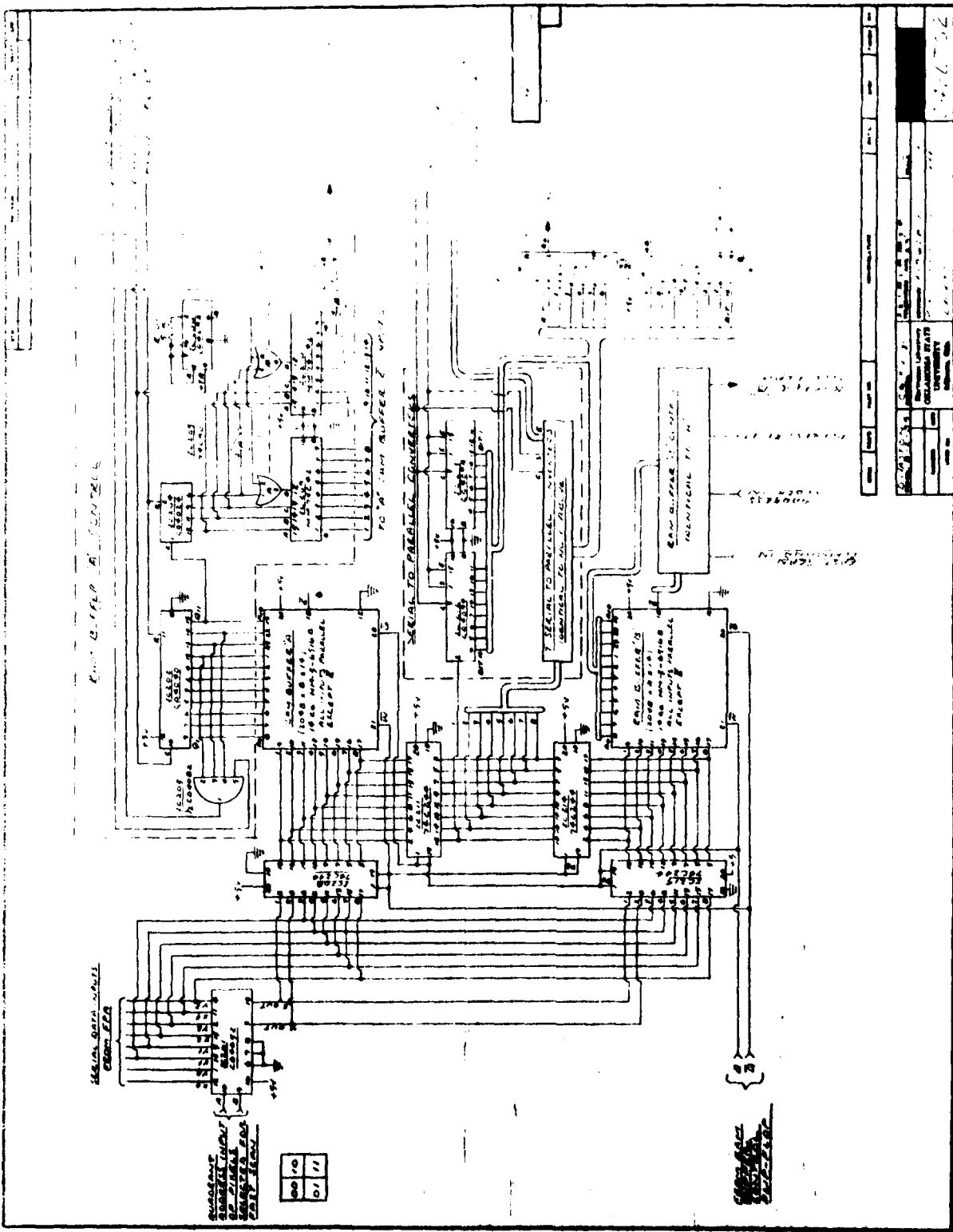
Each memory buffer contains eight 2048 x 8 RAM chips in parallel which are enabled in sequence to provide data storage for one complete pixel array scan. See Figure 4. The Q1 through Q11 outputs of a binary counter, IC 202, provides the RAM address inputs. The trailing edge of the Q11 output advances another binary counter every 2048 bits to enable the RAM's in sequence through two BCD-to-decimal decoder's, IC 209 and 210. The two decoders produce a logical zero at the output corresponding to a four bit binary input from zero to nine. For binary inputs from ten to fifteen all

outputs are high. The active output is transferred from IC 209 to IC 210 by the Q4 output of IC 204 through two OR gates to the "D" inputs of the decoders. Note that the "D" input to IC 210 is an inverted Q4 output. The second input to each OR gate is from a one-shot which is triggered by the bit clock to the RAM address counter. This provides a transition to the \bar{E} input of the active RAM after each address change. This is required by the RAM chip in order to latch the address in. Pin 7 of IC 210 goes low when RAM chip No 14 is full and thus provides a "BUFFER FULL" flag through inverters, IC205B, and OR gate, IC 207C.

2.4 Fast Scan Formatting

In the fast scan mode the system is designed to format into each minor frame the data from two scans of a selected 8 x 8 Array. See Figure 2. The quadrant address from which the data is taken is furnished from the FPA to the A & B inputs of IC 201. This switches the outputs of two selected A to D converters to inputs 1 & 2 of the active RAM buffer. A high at the command input of the formatter switches to the "fast-scan" operation. This applies a high to pin 5 of IC 203 which enables this gate for a "memory full flag" after one minor frame of data (896 bits from each of the two active converters) are stored. This high is also applied to pin 2 of IC 109 by holding Q of IC 108B high. This will allow data read to begin on the next minor frame by disabling the circuit used for major frame synchronization during normal scan. The command input also enables AND gate , IC 107D, to reset the counter, IC 116, on the "2" output so that data from the RAM buffers 1 & 2 only are clocked out. Note that the pixel readout is synchronized with the formatter minor frame sync through IC 117D during fast scan.





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